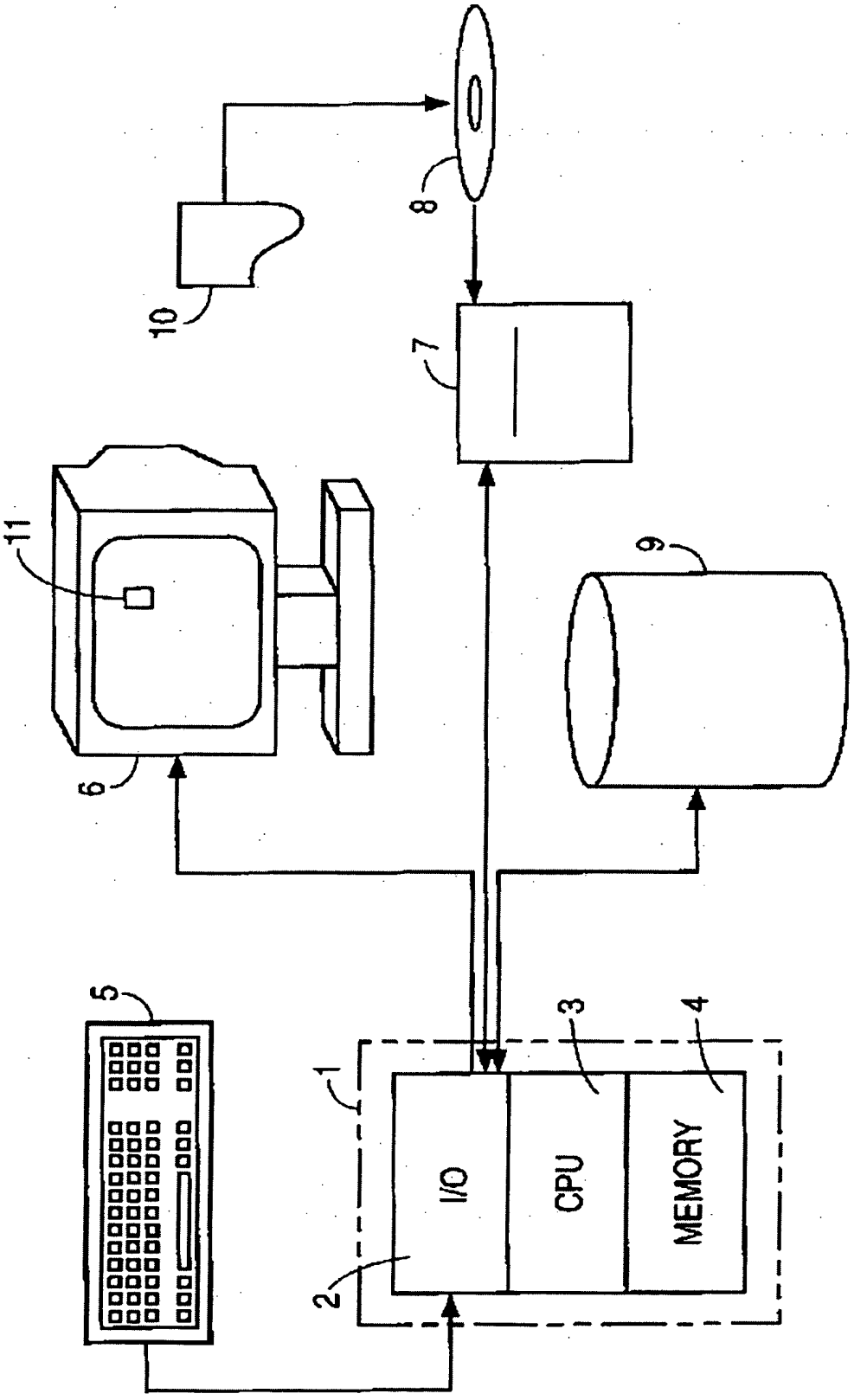

FIG. 1

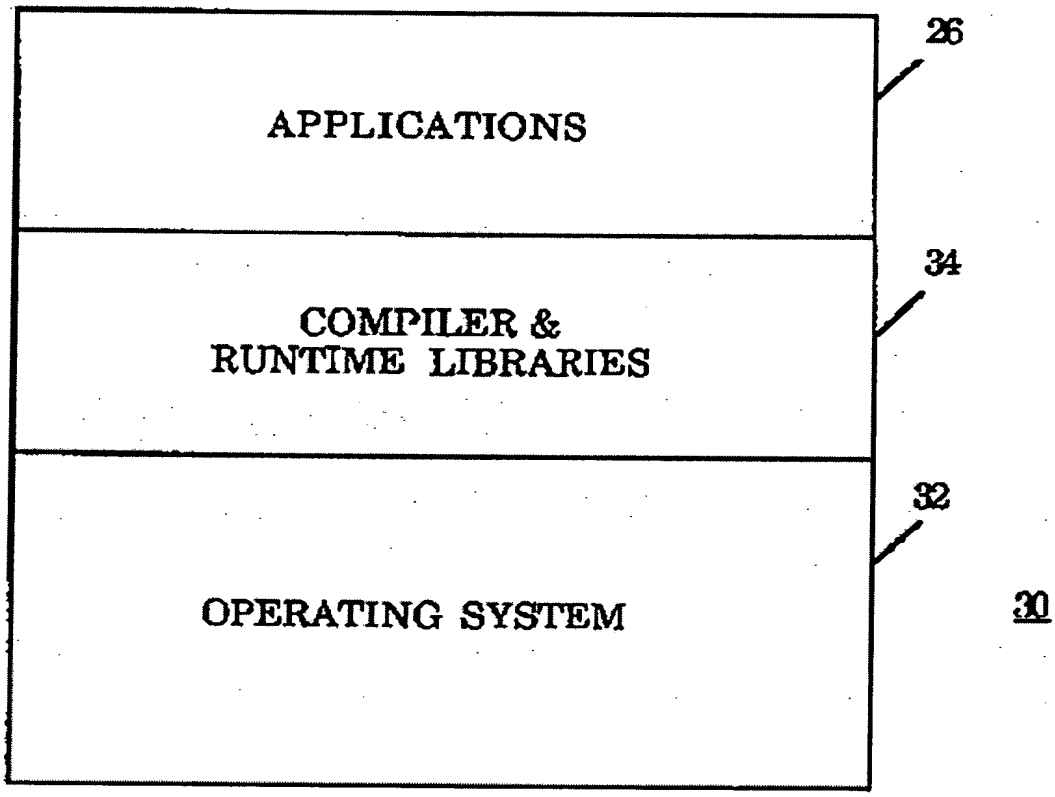
APPLICATIONS
26
COMPILER &
RUNTIME LIBRARIES
34
OPERATING SYSTEM
32
30

FIG. 2

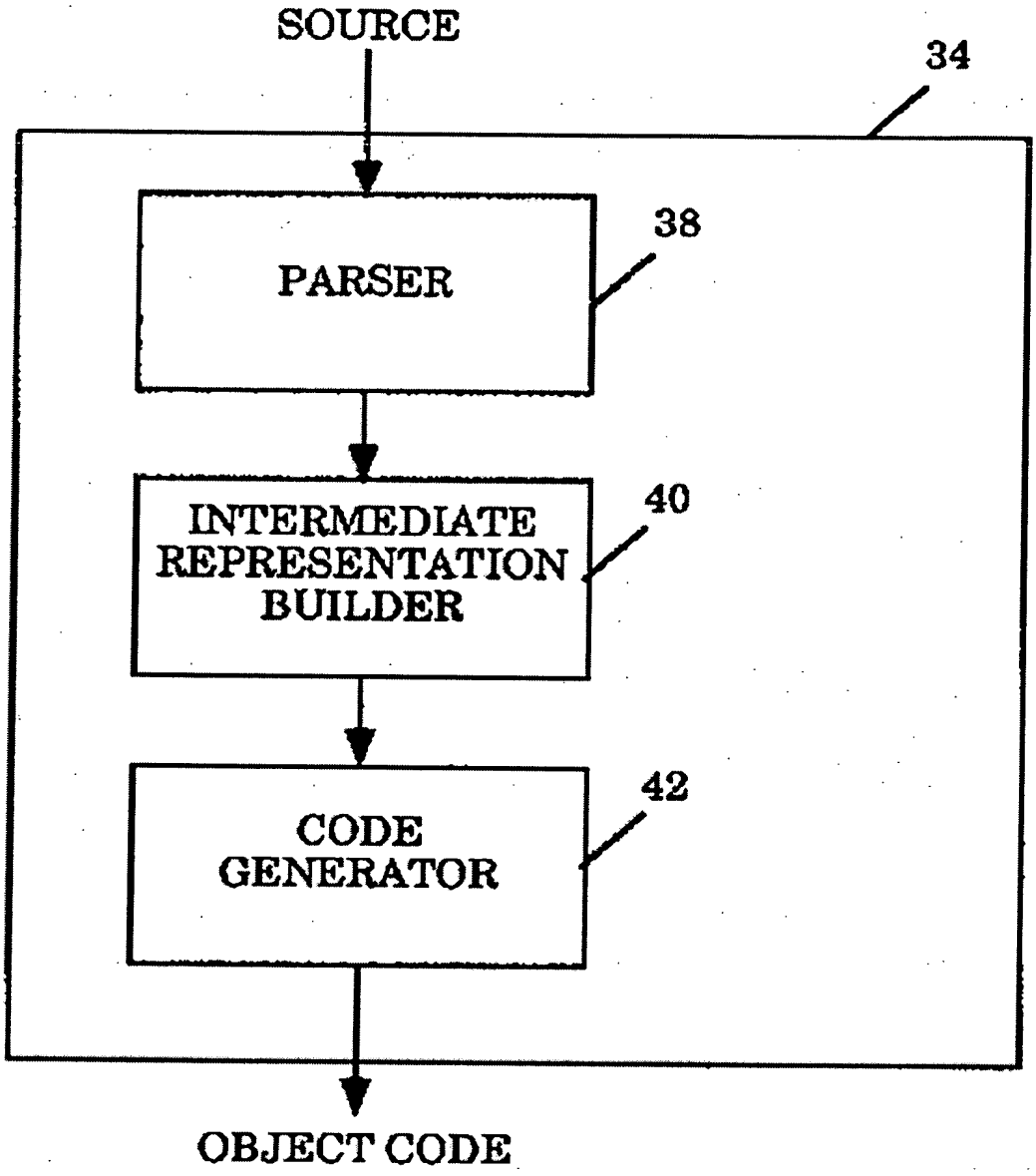
SOURCE
34
PARSER
38
INTERMEDIATE REPRESENTATION BUILDER
40
CODE GENERATOR
42
OBJECT CODE

FIG. 3a

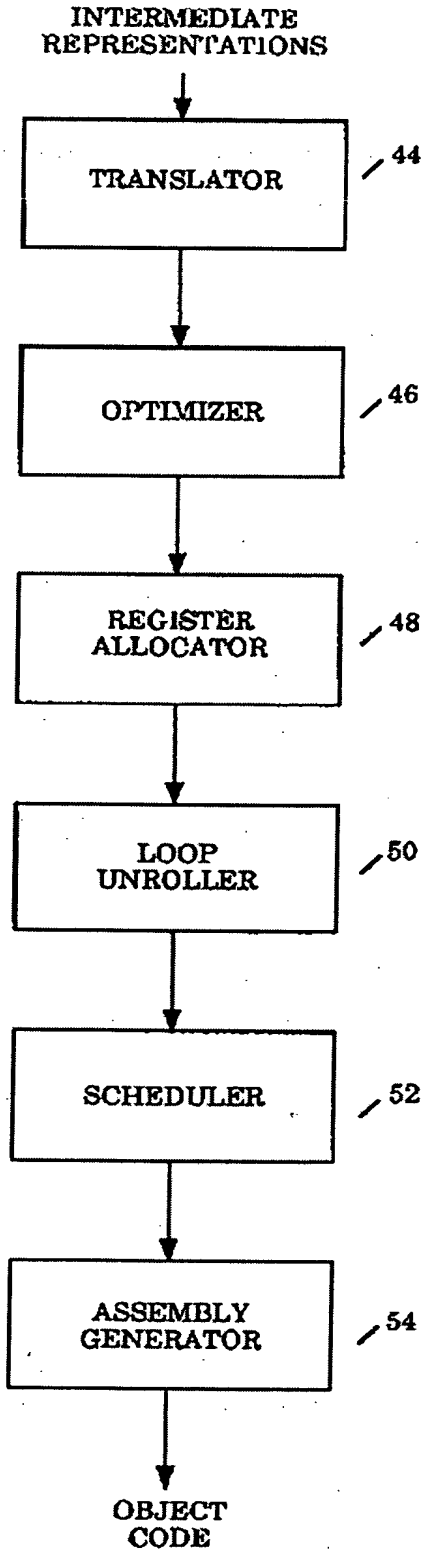
INTERMEDIATE REPRESENTATIONS
TRANSLATOR
44
42
OPTIMIZER
46
REGISTER ALLOCATOR
48
LOOP UNROLLER
50
SCHEDULER
52
ASSEMBLY GENERATOR
54
OBJECT CODE

FIG. 3b

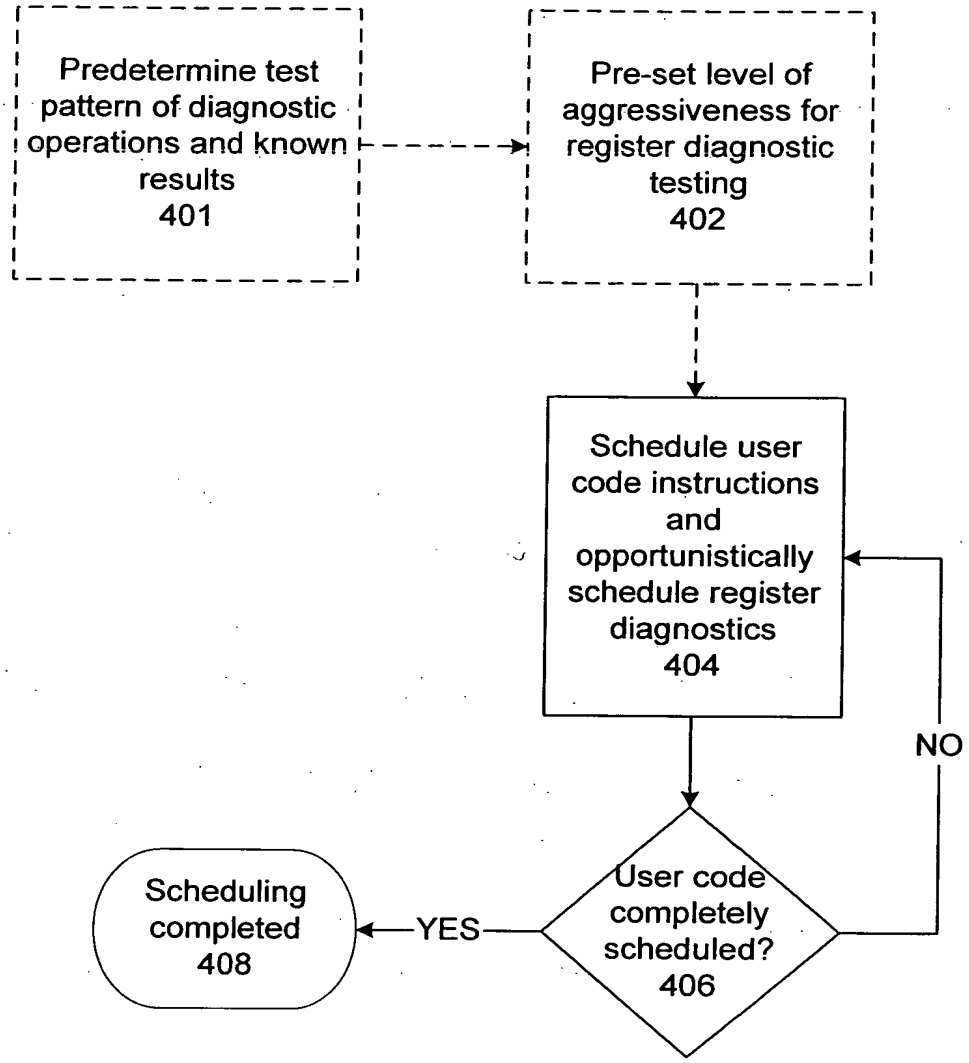
Predetermine test pattern of diagnostic operations and known results
401
Pre-set level of aggressiveness for register diagnostic testing
402
Schedule user code instructions and opportunistically schedule register diagnostics
404
User code completely scheduled?
406
NO
YES
Scheduling completed
408
400

FIG. 4

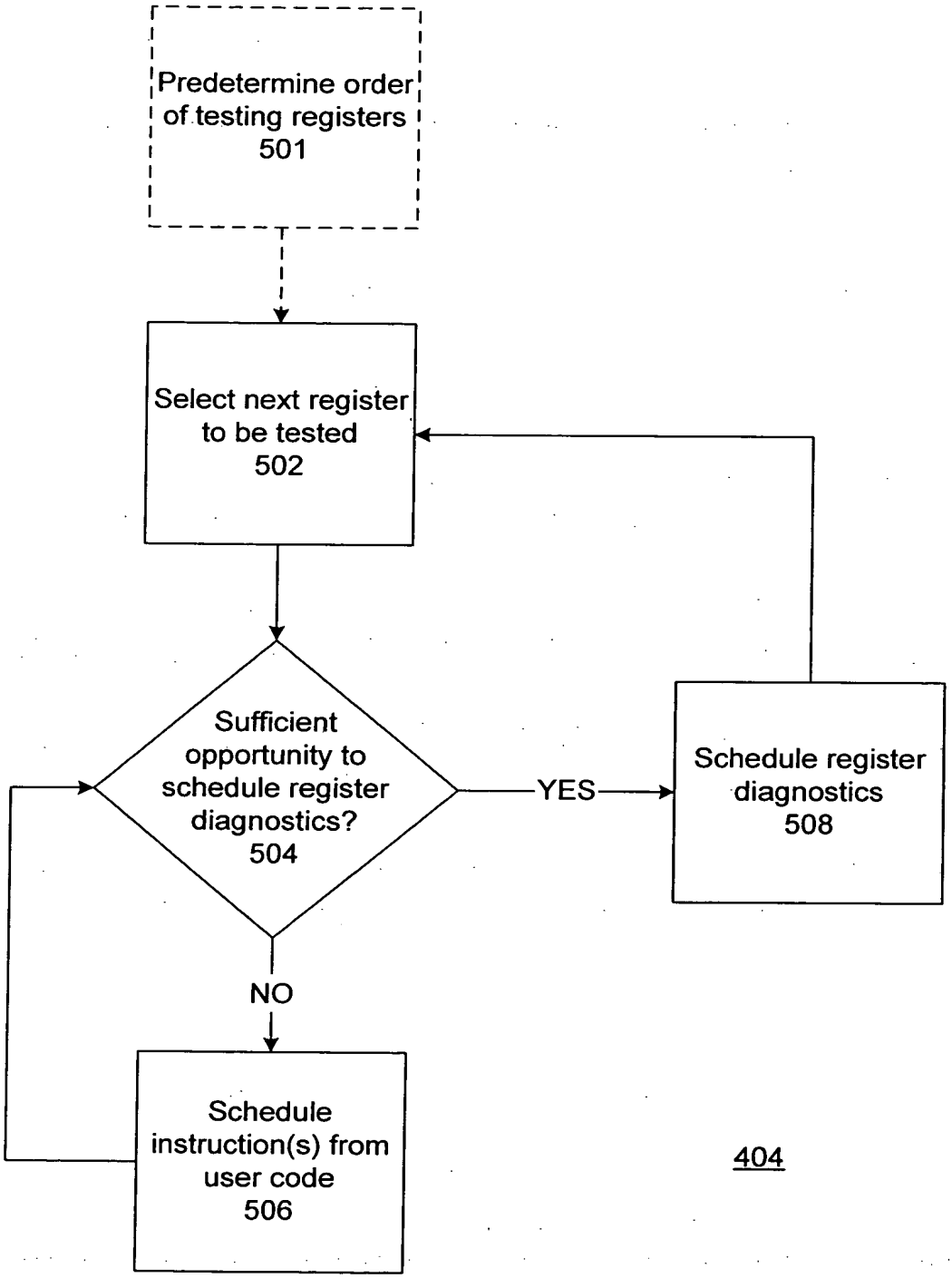
Predetermine order of testing registers 501
Select next register to be tested 502
Sufficient opportunity to schedule register diagnostics? 504
YES
Schedule register diagnostics 508
NO
Schedule instruction(s) from user code 506
404

FIG. 5

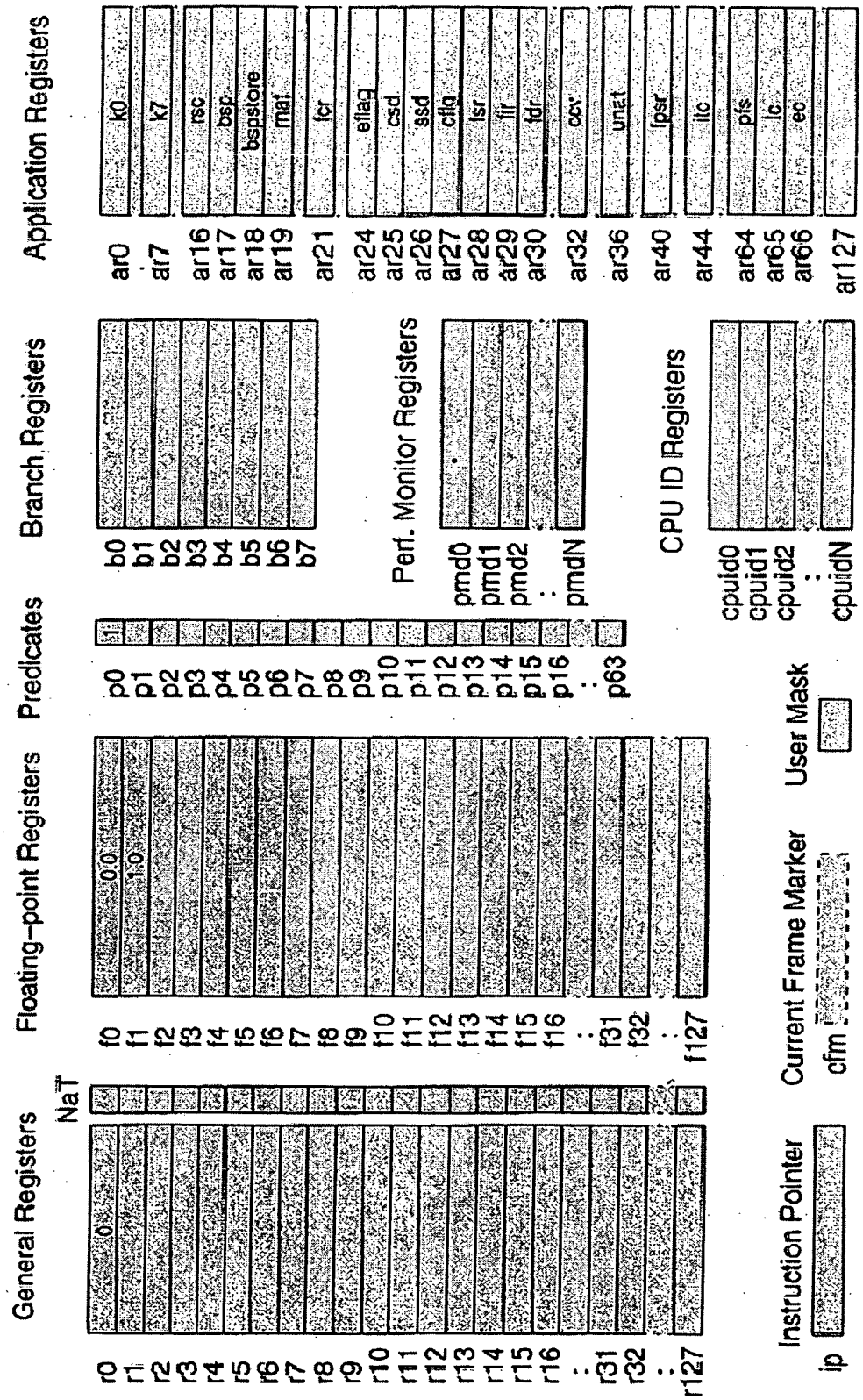
General Registers
NaT
Floating-point Registers
Predicates
Branch Registers
Application Registers
Perf. Monitor Registers
CPU ID Registers
Instruction Pointer
Current Frame Marker
User Mask
ip
cfm
r0 r1 r2 r3 r4 r5 r6 r7 r8 r9 r10 r11 r12 r13 r14 r15 r16 r31 r32 r127
f0 f1 f2 f3 f4 f5 f6 f7 f8 f9 f10 f11 f12 f13 f14 f15 f16 f31 f32 f127
p0 p1 p2 p3 p4 p5 p6 p7 p8 p9 p10 p11 p12 p13 p14 p15 p16 p63
b0 b1 b2 b3 b4 b5 b6 b7
pmd0 pmd1 pmd2 pmdN
cpuid0 cpuid1 cpuid2 cpuidN
ar0 ar7 ar16 ar17 ar18 ar19 ar21 ar24 ar25 ar26 ar27 ar28 ar29 ar30 ar32 ar36 ar40 ar44 ar64 ar65 ar66 ar127
k0 k7 rsc bsp bspstore rnat fcr eflag csd ssd cflg fsr fir fdr ccv unat fpsr itc pfs lc ec

FIG. 6
(Background Art)

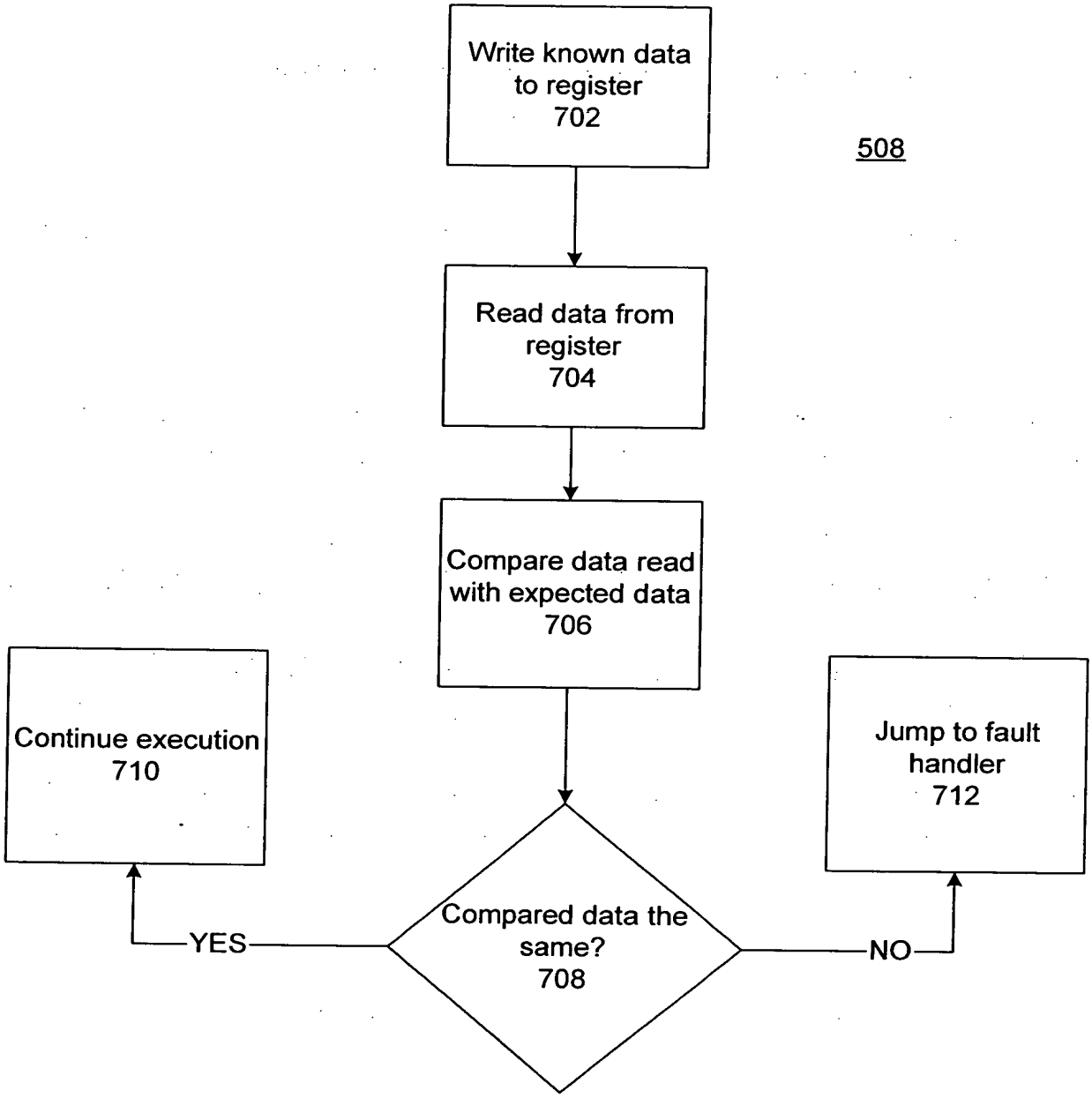
Write known data to register 702
508
Read data from register 704
Compare data read with expected data 706
Continue execution 710
Jump to fault handler 712
Compared data the same? 708
YES
NO

FIG. 7